Internal Representation and Behavioural Synthesis of Control Dominated Applications (1996) (Make Corrections) (3 citations)

Peeter Ellervee, Anshul Kumar, Bengt Svantesson, Ahmed Hemani ESD Lab, Dept. ...

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Abstract: In this paper we address problems encountered in behavioural synthesis of control dominated applications that are common in telecommunications. An internal representation, optimized for capturing control dominated behaviours and a synthesis strategy that takes into account the control flow is presented. Results of applying this strategy to realistic examples is presented and compared to commercial behavioural synthesis tools. 1. Introduction There are several applications which require ASICs... (Update)

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.... **how to map process structures from SDL into IRSYD [12] as well as a conceptual work for the internal representation of control flows [4].** Our intent is to present a generic mapping scheme to convert communication constructs from external languages into IRSYD in a consistent...

...proposed evolution of the AKKA design flow to AKKA , described in figure 32. **AKKA will use a graph based internal representation, XFC [29], to improve the hardware efficiency, estimations, and interface synthesis.** VHDL will be added as a front end language. FIGURE 33....

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ProGram: A Grammar-Based Method for Specification and Hardware.. - Öberg (1999) (Correct)
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  text = "P. Ellervee, A. Kumar, B. Svantesson, A. Hemani, Internal Representation
    and Behavioural Synthesis of Control Dominated Applications. The 14th NORCHIP
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using the well developed finite state machine (**FSM**) optimization techniques. Based on the ideas,
as a finite state machine which can be handled by an **FSM**/logic synthesis tool. In this paper, we present an
Figure 1. CMIST synthesis strategy Output **FSM** in **VHDL** /Verilog Extract Arithmetic Components Schedule /
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A Tool Converting Finite State Machine to **VHDL** Amr T. Abdel-Hamid, Mohamed Zaki and Sofi ene
www.ece.concordia.ca/~tahar/pub/CCECE04-FSM.pdf

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we present a framework for automated design of small **FSM** predictors for general purpose and customized
expression is then converted into a **FSM**. The **VHDL** for synthesis is then generated from the **FSM**.
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is described in **VHDL** as a network of interacting **FSM**Ds. In addition# it is assumed that the testability
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shrinking design times. Finite State Machines (**FSM**) are a fundamental building block in computer
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www-cse.ucsd.edu/~calder/papers/ISCA-01-FSM.ps

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by a finite state machine. Hence we use a **FSM** model as internal representation for state
for state extraction and scheduling. The **FSM** is a Moore type automaton. The internal
Processor Synthesis from Assembler Code using **VHDL** K. Tammemae, J. Udre Tallinn Technical University
www.ele.kth.se/%7Enalle/asiapap.ps.gz

Tools for mapping applications to CCMs - Mark Jones Michael (1998) (Correct)
inner product: A tree-structured graph with a small **FSM**, 4 adders and 4 multipliers The **FSM** is assigned to with a small **FSM**, 4 adders and 4 multipliers The **FSM** is assigned to the CPU and the adders/multipliers a DSP Select from a library or write from scratch **VHDL**, C, assembly, etc for each of the tasks (cells)
www.ccm.ece.vt.edu/papers//spie2.pdf

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